Dual WideBand Frequency Synthesizer with Integrated VCO and Loop Filter

Technical Data

CorePLL-1

FEATURES (for 2 PLLs)

- *3GPP superset LO sub-system (All bands + CA)*
- *PLL1 [0.49mm^2] for LTE with VCO1*
- *PLL2 [0.76mm^2] for LTE&GSM with VCO1 and VCO2*
- *Small size, high-performance and low-power (24mW)*
- *Various power and performance modes*
- *Power supply 1.35V and 1.8V*
- *Reference signal (FREF) from 10MHz to 400MHz*
- *Programmable reference divider (/1, /2, /4 & /8)*
- *Output RF signal (FOUT) from 1.333GHz up to 8GHz*
- *IQ Dividers (/2 & /4) for RX&TX down-to 333MHz*
- *Integrated loop filter with adjustable loop response*
- *Integrated bandgap reference and LDOs*
- *SPI control bus (IO) and test IO*
- *Digital calibrations and lock detection*
- *Fast settling <100us*
- *Package: QFN6x6-48 or 2.4mm x 3.6mm RDL Fan-In*

GENERAL DESCRIPTION

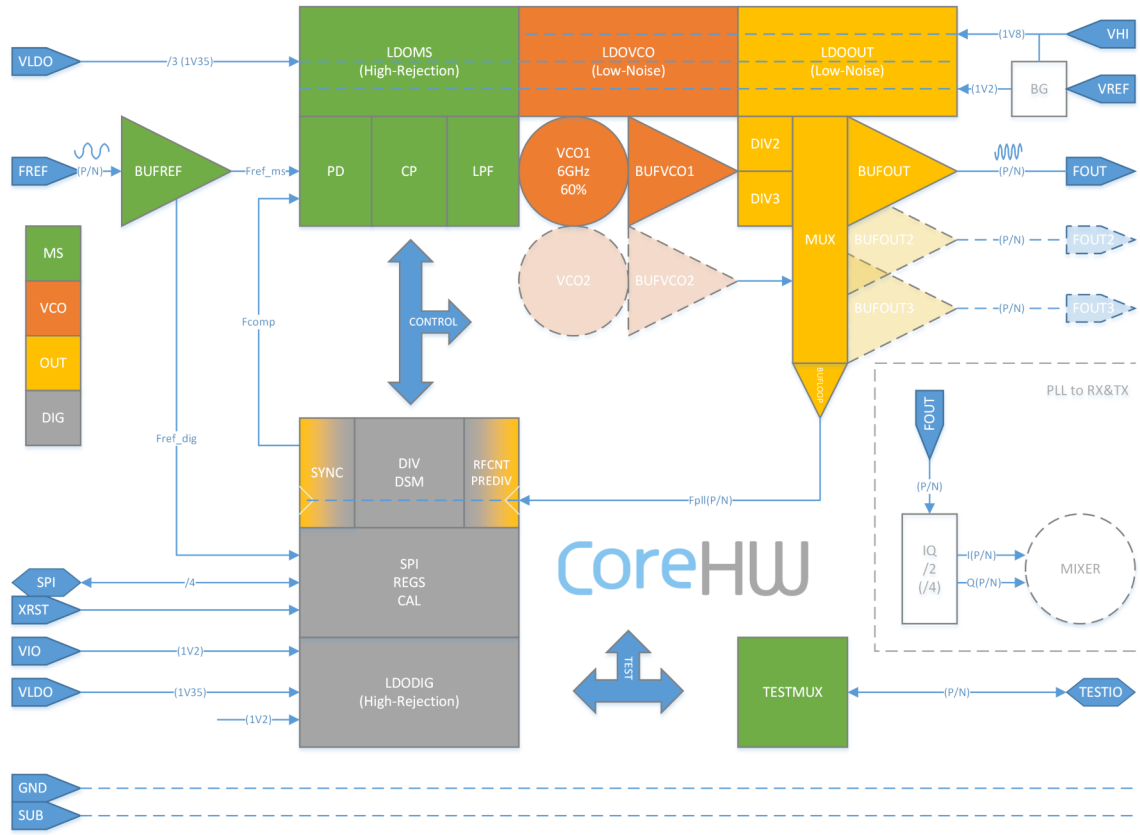
CorePLL is a wideband phase-locked loop (PLL) system for 2G (GSM) 3G and 4G (LTE), including Carrier Aggregation (CA) for 3GPP Rel11 and Rel12. CorePLL frequency synthesis sub-system enables single transceiver LTE CA. CorePLL consists of two fully integrated PLLs with integrated VCOs and loop filters. CorePLL is versatile frequency synthesizer solution with small size, high-performance and ultra low-power. Power consumption is only 18mA from 1.35V supply (24mW). CorePLL supports variety of different systems and reference clock frequencies. CorePLL is implemented using standard 55nm CMOS process. CorePLL is available in QFN 6x6mm package. PLL1 and PLL2 synthesizers are also available as IPs.

www.corehw.com

APPLICATIONS

Wireless Systems (GSM, WCDMA, LTE Rel11 and Rel12 with inter and intra band Carrier Aggregation)
WLAN, Bluetooth, Automotive, Industrial

BLOCK DIAGRAM



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